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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/779,209 | 02/08/2001 | Michael S. Allen | A0312/7379(RMA) | 6630 |

23628 7590 01/14/2005

WOLF GREENFIELD & SACKS, PC
FEDERAL RESERVE PLAZA
600 ATLANTIC AVENUE
BOSTON, MA 02210-2211

| EXAMINER | |
|---|---|
| FLEMING, FRITZ M | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2182 | |

DATE MAILED: 01/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/779,209 | ALLEN ET AL. | |
| | Examiner | Art Unit | |
| | Fritz M Fleming | 2182 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-56* is/are pending in the application.

4a) Of the above claim(s) *18-32,40-46 and 48-56* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17,33-39 and 47* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

FRITZ FLEMING
PRIMARY EXAMINER
GROUP 2100

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 May 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. Applicant's election with traverse of Group I claims 1-17,33-39,47 in the reply filed on 10/13/2004 is acknowledged. The traversal is on the ground(s) that the search for the different claim groups would be co-extensive. This is not found persuasive because the different claim groups represent different variations and hence present numerous subcombinations usable together, which was not argued by applicants.

The requirement is still deemed proper and is therefore made FINAL.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-8,14,15,33-35,37-39,47are rejected under 35 U.S.C. 102(b) as being anticipated by Windrem et al.

For claim 47, a cache memory system is shown in Figure 1. A plurality of locations in the cache 14 store data and addresses associated with the data (per column 6, lines 5-11 that show cache addresses for location of video and audio materials that are needed for playback or providing the address necessary to indicate where newly recorded material will be placed in the cache prior to transfer to the disk. Means for accessing memory locations of the cache independently of a cache controller that controls access to memory of the cache by a processor are seen as the independent disk controllers 13, each having an independent DMA controller that independently perform direct memory

access transfers between cache 14 and the individual disk drives 17. The DMA engines are equivalent to an embodiment encompassed by applicants, hence anticipation is proper. Note that the cache 14 appears to be a single common memory to the control 99 and appears to be an independent memory to each disk controller.

For claim 33, an associative cache is accessed per the addressing above, with the DMA access of each disk drive 13 being independent of other controllers such as redundant data control 99, which sees the cache as a single common memory. Each disk controller has an independent DMA controller (hence engine) that transfers data in a DMA manner between a lower level memory in the disk drive 17 to the cache 14 and vice versa (claims 34 and 35). For claims 37-39, it is to be noted that a DMA transfer is address based, and hence per column 2, lines 60+, as the large blocks of data are to be transferred between the disks and cache by the DMA controllers transferring smaller blocks, with DMA reprogramming mentioned at the top of column 3. Thus the use of block transfers requires and hence anticipates the use of addresses at both the cache and disks to ensure the proper transfer of the data blocks. As far as the incrementing or decrementing of addresses is concerned, it is to be noted that contiguous data on each disk drive 17 can be transferred to and from non-contiguous cache locations (Figure 2 and column 3, lines 1-12), and data stored in the cache is stored in video block and audio block sections (column 3, lines 50+), such that an element 20 from a disk corresponds to two cache blocks. Note also that per column 9, lines 46+, that continuous data can be written to or supplied from a series of non-continuous access disks, wherein per column 3, lines 28-49, audio and video data can be separately

manipulated such as video recorded while audio is played. Thus the ability to transfer continuous data to and from non-continuous locations sets forth the ability to increment/decrement in either first/second address sets without doing so at the other. Thus the ability to do such a transfer will require addresses to be incremented and/or decremented in different values, depending on where the continuous data is and where the non-continuous data is. Per claims 1-8 and 15, the cache 14 has the memory locations, and the first and second controllers are in the form of the DMA controllers that access the cache locations by the associated devices, being the devices are the disk controllers, making the DMA engines the claimed controllers and the disk controllers the claimed devices. Data is transferred between the lower memory in the form of the disk drives and the cache. Claims 6-8 are parallel to claims 37-39, and are rejected for the same reasons. It is also to be pointed out that the cache 14 consists of multiple dual ported memories. Claim 14 is met by a third controller 16 that is the system controller which governs stop, play, record, and managing cache 14 and disk read and write, thus arbitrating access to the cache 14 which appears to the control 99 as a single common memory.

### *Claim Rejections - 35 USC § 103*

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 9-13,16,17,36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Windrem et al. in view of the admitted prior art.

Windrem does not specifically mention the common die, the single word line, the address inputs, the multiplexers, and the DSPs for the processors.

The admitted prior art sets forth the well-known use of DSPs with integrated cache (page11, line 30), which is indicative of use of a single die for a processor and cache. Single line words are mentioned at page 4 as being commonly used to exploit locality as well as implementation of replacement policies. Multi-port memories are mentioned at

page 3. Multiplexers in the admitted prior art are shown at 218,220,222,224,226,230,238 wherein decoder 206 uses an incoming address selected by multiplexer 218 (from either 112a or 114a or 118a) and in a similar manner, the output address is selected at 230a in order to provide the address 120a for a memory store address.

Therefore it would have been obvious to one having ordinary skill in the art at the time that the invention was made to modify Windrem et al. by the teachings of the admitted prior art in order to be able to integrate the controllers on a common die, so as to provide the ability to integrate cache with a processor, and thus combine controllers with their caches in an integrated manner. As far as the use of DSPs is concerned, the admitted prior art states that these are being used in order to simplify the general programming model and improve competitiveness, thereby providing rationale to modify Windrem et al. to use DSPs as the controllers for the same reasons. As far as the single line word is concerned, the admitted prior art states that this is common to exploit locality as well as replacement policies, both of which are used in Windrem et al., such as the retrieval or storage policy per column 4, lines 59+. As far as the multiplexers of claims 11-13 are concerned, the admitted prior art teaches multiplexers to select input and output addresses. AS far as the particular selection input are concerned, it is to be noted that Windrem et al. does teach the ability to select video recording while audio playback or playing video while skipping the audio. AS the cache is divided into video and audio blocks and random access to data stored in the disk array 12 is allowed, then the ability to select an address input from either of the controllers/DMA engines and

external address of the disk array for the output multiplex is rendered obvious by the ability of Windrem et al. to be able to use the multi-port cache memories of the cache 14 in such a manner so as to allow the independent DMA transfers between the cache and disks in a concurrent manner as suggested by the prior art on page 3, in order to reduce bank busy times.

***Conclusion***

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. IBM TDB shows a shared cache with multiple processors. EP 0507066 shows a shared L2 with independent processors. Shih shows a global cache 20 with LRU 34. Braceras et al. show multiplexers 80 and 82. Kalish et al. show independent cache controllers 30,31. Mohrman et al. show a cache 12 with two independent control processors. Lau shows a CPU 101 and DMA 104 and cache 102 with controller 200. Stevens shows a shared cache with multiple processors and EP 0637799 shows multiple processors 3 with a shared interleaved cache unit 100 and controller 10.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fritz M Fleming whose telephone number is 571-272-4145. The examiner can normally be reached on M-F, 0600-1500.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey Gaffin can be reached on 571-272-4146. The fax phone number for the organization where this application or proceeding is assigned is 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Fritz M Fleming
Primary Examiner
Art Unit 2182

fmf